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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,263	05/31/2001	Kenneth Lerman	SYCS-035	4732

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EXAMINER	
MCCARTHY, CHRISTOPHER S	

ART UNIT	PAPER NUMBER
2113	9

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,263	LERMAN, KENNETH	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 7-20 and 23 is/are allowed.

6)☒ Claim(s) 1-6,21 and 22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 5/31/2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 21,22 are rejected under 35 U.S.C. 102(b) as being anticipated by Gammukhi et al U.S. Patent 5,953,314.

As per claim 1, Gammukhi teaches that in a computer system, said system including a plurality of system control processors, each said system control processor with a plurality of activation states, said system control processors controlling a plurality of other processors (OPs) in said system, each said OP with a plurality of activation states (column 1, lines 53-59; figure 1), a method, comprising the steps of: providing a reset function for said system control processors enabling said system control processors to change the activation state of other system control processors and OPs (column 5, lines 39-40; column 2, lines 52-55); setting the activation state of a system control processor to active, said active state indicating a functioning processor fully integrated into system operations (column 3, lines 37-42); setting the activation state of a system control processor to standby, said standby activation state indicating a functioning processor partially integrated into said system operations (column 2, lines 52-55; column 3, lines 37-42); detecting an error in one of said OPs with said system control processor set to an active activation state; detecting said error in one of said OPs with said system control processor set to a standby activation state; and altering the activation state of said OP using said system control

processor set to an active activation state and said system control processor set to a standby activation state (column 2, lines 52-65).

As per claim 2, Gammukhi teaches the method of claim 1, comprising the further step of: changing the activation state in the OP in which an error was detected from an active state to a reset state, said reset state indicating a non-functioning processor not integrated into said system operations (column 2, lines 52-55; column 5, lines 39-40).

As per claim 3, Gammuhki teaches the method of claim 2, comprising the further step of: changing the activation state of an OP from a standby activation state to an active activation state to take the place in said system of said OP placed into a reset activation state (column 2, lines 12-21).

As per claim 4, Gammuhki teaches the method of claim 1, wherein said OPs are located on Input/Output (IO) cards interfaced with said system, said IO cards including software for reporting IO card status and OP status to said system control processor set to an active activation state and said system control processor set to a standby activation state (column 2, lines 52-55).

As per claim 5, Gammuhki teaches the method of claim 4, wherein said error is detected by said software and reported to said system control processor set to an active activation state and said system control processor set to a standby activation state (column 5, lines 52-55).

As per claim 6, Gammuhki teaches the method of claim 5, wherein said error is detected by polling said OPs to check status (column 2, lines 52-65).

As per claim 21, Gammukhi teaches an electronic device comprising: a system control processor set to an active activation state, said active activation state indicating a functioning processor fully integrated into the operations of said device (column 3, lines 37-42)); a system

control processor set to a standby activation state, said standby activation state indicating a functioning processor partially integrated into the operations of said device (column 2, lines 52-55); a plurality of other processors (OPs) with a plurality of activation states, said OPs controlled by said system control processors, wherein an error in one of said OPs is detected by said system control processor set to an active activation state, said error is verified by said system control processor set to a standby activation state (column 2, lines 52-65), and said system control processors change the activation state of the OP with an error to a reset activation state, said reset activation state indicating a non-functioning processor not integrated into the operations of the device (column 2, lines 52-65).

As per claim 22, Gammukhi teaches that in a computer system, said system including a plurality of system control processors, each said system control processor with a plurality of activation states, said system control processors controlling a plurality of other processors (OPs) in said system, each said OP with a plurality of activation states (column 1, lines 53-59; figure 1), a method, comprising the steps of: providing a reset function for said system control processors enabling said system control processors to change the activation state of other system control processors and OPs (column 5, lines 39-40; column 2, lines 52-55); setting the activation state of a system control processor to active, said active state indicating a functioning processor fully integrated into system operations (column 3, lines 37-42); setting the activation state of a system control processor to standby, said standby activation state indicating a functioning processor partially integrated into said system operations (column 2, lines 52-55; column 3, lines 37-42); detecting an error in one of said OPs with said system control processor set to an active activation state; detecting said error in one of said OPs with said system control processor set to

a standby activation state; and altering the activation state of said OP using at least one of said system control processor set to an active activation state and said system control processor set to a standby activation state (column 2, lines 52-65).

Allowable Subject Matter

3. Claims 7-20, 23 are allowed.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance: When read as a whole, claims 7, 10, 17, and 23 are allowable with respect to the following limitations:

As per claims 7 and 17, the primary reason for allowance is the limitation of failing to detect said error in one of said OPs with said system control processor set to a standby activation state.

As per claim 10, the primary reason for allowance is the limitation of altering the activation state of said system control processor set to an active activation state using said system control processor set to a standby activation state and said system component with a reset function.

As per claim 23, the primary reason for allowance is the limitation of attempting and failing to verify said error in said system control processor set to an active activation state with said system component with a reset function.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please refer to attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (703)305-7599. The examiner can normally be reached on M-F, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703)305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
March 12, 2004

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